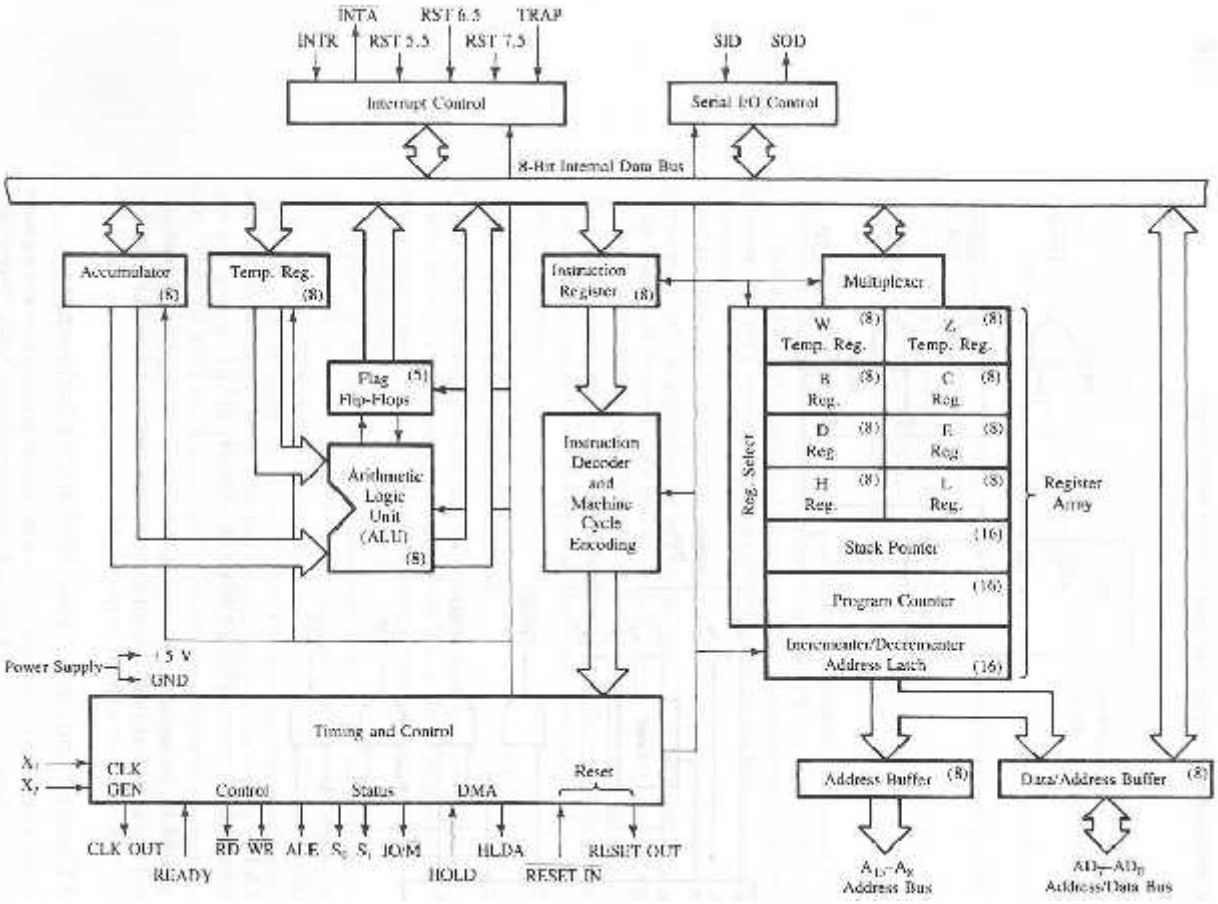
(1) Draw and explain the internal architecture of 8085.

- The architecture of 8085 Microprocessor is shown in figure given below. The internal architecture of8085 includes following section
  ALU-Arithmetic and Logic
  unitTiming and control unit
  Instruction register and
  decoder,Register array,
  Interrupt control and serial I/O control.



ALU:-

The ALU performs the arithmetic and logical operations. The operations performed by ALU of 8085 are addition, subtraction, increment, decrement, logical AND, OR, EXCLUSIVE -OR, compare, complementand left / right shift. The accumulator and temporary register are used to hold the data during anarithmetic / logical operation. After an operation the result is stored in the accumulator and the flags are set or reset according to the result of the operation.

TIMING & CONTROL UNIT:

The timing and control unit synchronizes all the microprocessor operations with the clock and generatesthe control signals necessary for communication between the microprocessor and peripherals.

INSTRUCTION REGISTER & DECODER:

When an instruction is fetched from memory it is placed in instruction register. Then it is decoded and encoded into various machine cycles.

REGISTER ARRAY:

Apart from Accumulator (A-register), there are six general-purpose programmable registers B, C, D, E, Hand L. They can be used as 8-bit registers or paired to store l6-bit data. The allowed pairs are B-C, D-Eand H-L.

The temporary registers W and Z are intended for internal use of the processor and it cannot be used by the programmer.

STACK POINTER (SP):

The stack pointer SP, holds the address of the stack top. The stack is a sequence of RAM memory locations defined by the programmer. The stack is used to save the content of registers during the execution of a program.

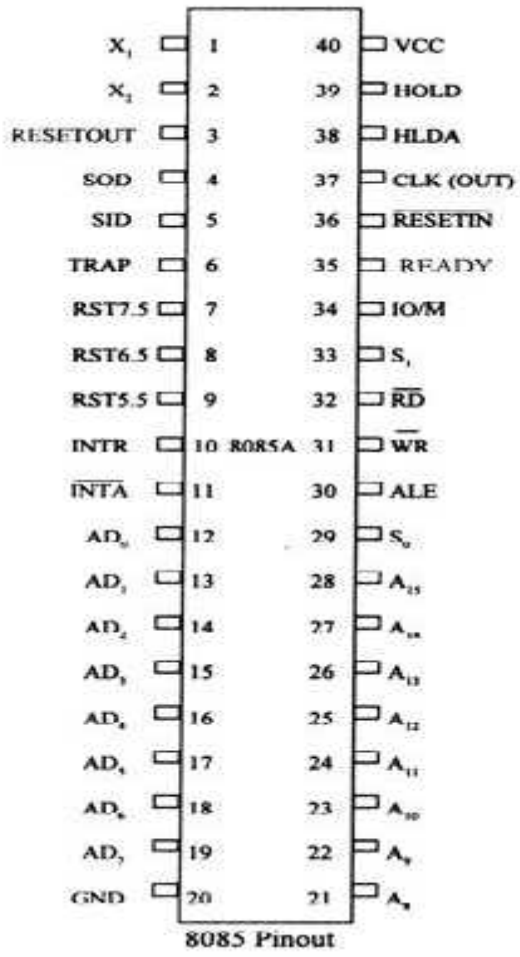
PROGRAM COUNTER (PC):

The program counter (PC) keeps track of program execution. To execute a program the starting address ofthe program is loaded in program counter. The PC sends out an address to fetch a byte of instruction from memory and increment its content automatically. Hence, when a byte of instruction is fetched, the PC holds the address of the next byte of the instruction or next instruction.

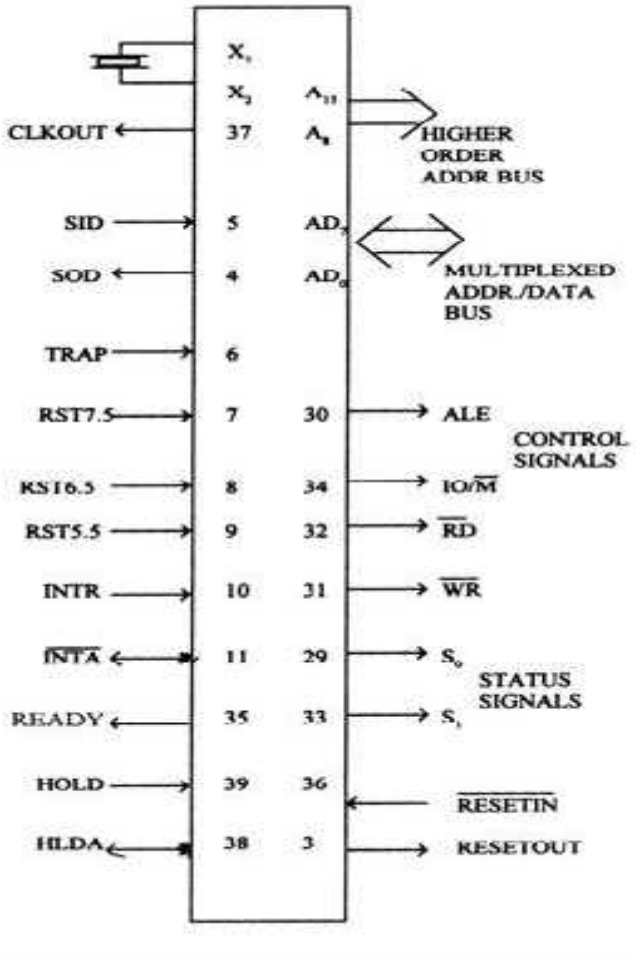
INTERRUPT CONTROL:-interrupt control provide control for following interrupt INT, INTA, RST5.5,RST6.5, RST7.5, TRAP

SERIAL I/O CONTROL: IT provide two pin for serial communication SOD-Serial output data and SID-
Serial input data

(2) Draw the PIN DIAGRAM of 8085 & explain the detail of each pin OR Draw & explain 8085 Pin out signals OR Explain function of HOLD and HLDA pin in brief OR List the function of flowing pins of 8085 (i) ALE, (ii) CLK (iii) Ready OR List the interrupt pins of 8085.



8085 Pinout



X1 & X2

These are also called Crystal Input Pins. 8085 can generate clock signals internally. To generate clocksignals internally, 8085 requires external inputs from X1 and X2.

RESET IN:

It is used to reset the microprocessor. It is active low signal. When the signal on this pin is low (for atleast 3 clocking cycles), it forces the microprocessor to reset itself.
Resetting the microprocessor
means:Clearing the PC and IR.
Disabling all interrupts (except TRAP).
Disabling the SOD pin.
All the buses (data, address, control) are
tristated.Gives HIGH output to RESET OUT
pin.

RESET OUT:

It is used to reset the peripheral devices and other ICs on the circuit. It is an output signal. It is an active high signal. The output on this pin goes high whenever RESET IN is given low signal. The output remains high as long as RESET IN is kept low

SID (Serial Input Data):

It takes 1 bit input from serial port of 8085 and Stores the bit at the 8^{th} position (MSB) of the Accumulator.RIM (Read Interrupt Mask) instruction is used to transfer the bit.

SOD (Serial Output Data):

It takes 1 bit from the 8^{th} position (MSB) of the Accumulator to serial port of 8085. SIM (Set Interrupt Mask) instruction is used to transfer the bit.

Interrupt Pin:

TRAP:-
It is a non-maskable interrupt. It has the highest priority. It cannot be disabled. It is both edge and level triggered. It means TRAP signal must go from low to high and must remain high for a certain period of time. TRAP is usually used for power failure and emergency shutoff.

RST 7.5:-
It is a maskable interrupt. It has the second highest priority. It is positive edge triggered only. The internalflip-flop is triggered by the rising edge. The flip-flop remains high until it is cleared by RESET IN.

RST 6.5:-

It is a maskable interrupt. It has the third highest priority. It is level triggered only. The pin has to be held high for a specific period of time.RST 6.5 can be enabled by EI instruction. It can be disabled by DI instruction.

RST 5.5:-

It is a maskable interrupt. It has the fourth highest priority. It is also level triggered. The pin has to be heldhigh for a specific period of time. This interrupt is very similar to RST 6.5.

INTR:-

It is a maskable interrupt. It has the lowest priority. It is also level triggered. It is a general purpose interrupt. By general purpose we mean that it can be used to vector microprocessor to any specific subroutine having any address.

INTA:

It stands for interrupt acknowledge. It is an outgoing signal. It is an active low signal. Low output on this pin indicates that microprocessor has acknowledged the INTR request.

Address and Data Pins

AD0 – AD7:- (Bidirectional)

These pins have dual purpose of transmitting lower order address and data byte. During 1st clock cycle, these pins act as lower half of address. In remaining clock cycles, these pins act as data bus. The separation of lower order address and data is done by address latch.

A8 – A15:-(Unidirectional)

These pins carry the higher order of address bus. The address is sent from microprocessor to memory.

ALE:- (Output)

It is used to enable Address Latch. It indicates whether bus functions as address bus or data bus.If ALE = 1 then Bus functions as address bus.

If ALE = 0 then Bus functions as data bus.

S0 and S1 :-(output)

S0 and S1 are called Status Pins. They tell the current operation which is in progress in 8085.

S0	S1	Operation
0	0	Halt
0	1	Write
1	0	Read
1	1	Opecode

IO/M:-

This pin tells whether I/O or memory operation is being performed.If IO/M = 1 then I/O operation is being performed.
If IO/M = 0 then Memory operation is being performed.

RD:-

RD stands for Read. It is an active low signal. It is a control signal used for Read operation either from memory or from Input device. A low signal indicates that data on the data bus must be placed either from selected memory location or from input device.

WR:-

WR stands for Write. It is also active low signal. It is a control signal used for Write operation either into memory or into output device. A low signal indicates that data on the data bus must be written into selected memory location or into output device.

READY:-

This pin is used to synchronize slower peripheral devices with fast microprocessor

HOLD:-

HOLD pin is used to request the microprocessor for DMA transfer. A high signal on this pin is a request to microprocessor to come off from the hold on buses. This request is sent by DMA controller.

HLDA:-

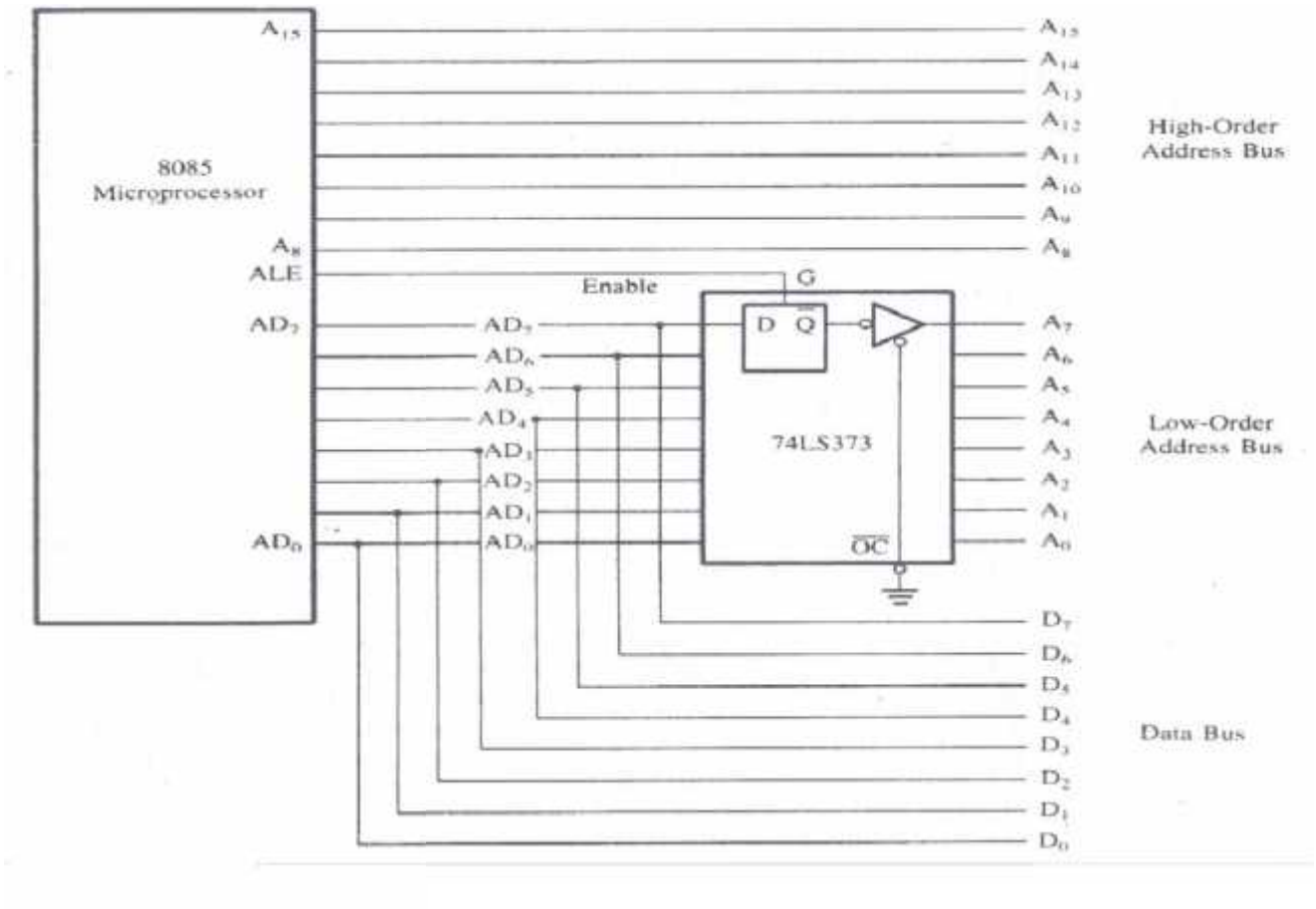
HLDA stands for Hold Acknowledge. The microprocessor uses this pin to acknowledge the receipt of HOLD signal. When HLDA signal goes high, address bus, data bus, RD',WR', IO/M' pins are *tri-stated*. This means they are cut-off from external environment. The control of these buses goes to DMAController.

VSS and VCC:-

+5V power supply is connected to VCC. Ground signal is connected to VSS.

(3) Explain how to demultiplex address from multiplex address/Data line. OR Describe Demultiplexed address data bus and control signals.

- AD0- AD7 lines are use for dual purpose i.e. Address bus and Data bus and they need to be demultiplexed to get all the information.
- The high order bits of the address remain on the bus for three clock periods. However, the low order bits remain for only one clock period and they would be lost if they are not saved externally.
- To make sure we have the entire address for the full three clock cycles, we will use an external latch tosave the value of AD7–AD0 when it is carrying the address bits. We use the ALE signal to enable this latch.



- The address AD7 –AD0 is connected as inputs to the latch 74LS373.
- The ALE signal is connected to the enable (G) pin of the latch and the OC –Output control –of thelatch is grounded
- ALE operates as a pulse during T1, when this signal goes low, the address is saved and the AD7-AD0lines can be used for data bus.

(4) Explain flag register of 8085.

- Flag is flip-flops that indicate some condition produce by the arithmetic and logical instruction. This flip-flop can set or reset according to the result of an operation.
- These flags are Zero (Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags.
- The bit position for the flags in flag register is,

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	X	AC	X	P	X	CY

Sign Flag:-After execution of any arithmetic and logical operation, if D7 of the result is 1, the sign flag is set. Otherwise it is reset

Zero Flag:-This flag is set if result obtained after an operation is 0.and Reset if Result is non Zero.
Carry Flag:-This flag is set if there is a carry or borrow from arithmetic operation.
Auxiliary Carry Flag: -This flag is set if there is a carry out of bit 3.
Parity Flag:-This flag is set if parity is even (even numbers of 1s) and reset if parity is odd(odd numbers of 1s).

(5) Discuss the bus organization of 8085.

The 8-bit 8085 CPU (or MPU – Micro Processing Unit) communicates with the other units using a 16-bit address bus, an 8-bit data bus and a control bus.

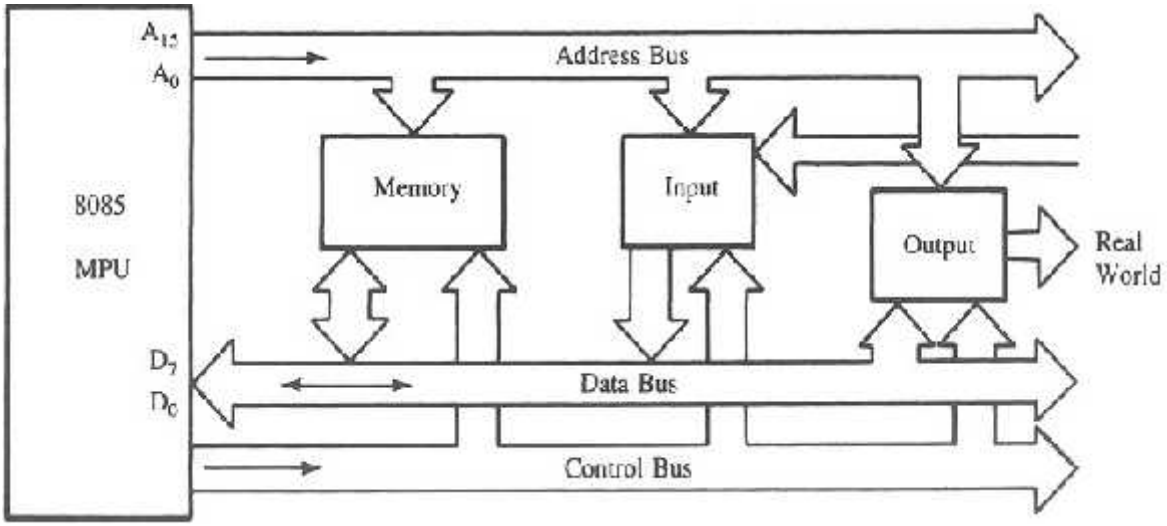
Address Bus

It consists of 16 address lines: $A_0 – A_{15}$

It operates in **unidirectional** mode: The address bits are always sent from the MPU to peripheral devices in one direction, not reverse.

MPU uses the address bus to perform first function : identifying a peripheral or a memory location.16 address lines are capable of addressing a Total of 2^{16}=65,536 (64k) memory locations.
Address locations: 0000 (hex) to FFFF (hex)

When the 8085 wants to access a peripheral or a memory location, it places the 16-bit address on the address bus and then sends the appropriate control signals.



Data Bus

It consists of 8 data lines: $D_0 – D_7$

It operates in **bidirectional** mode: The data bits are sent from the MPU to peripheral devices, as well as from the peripheral devices to the MPU.

The MPU uses the data bus to perform second function : Transfer binary information (data and instructions)

Data range: 00 (hex) – FF (hex)

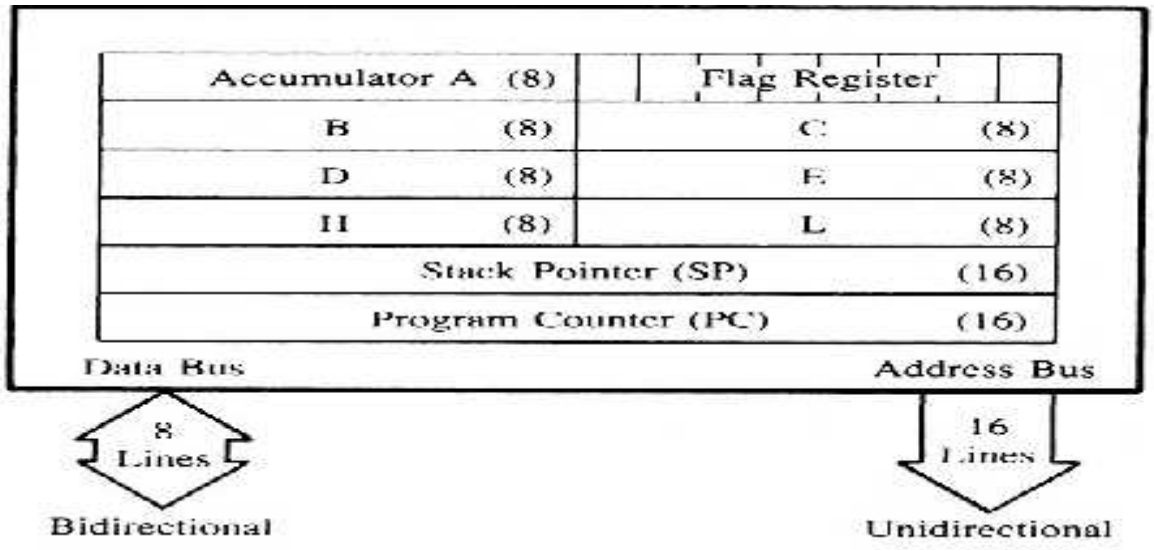
Control Bus

It comprised of various single lines that carry synchronization signals.

The MPU uses such lines to perform third function: Provide timing or synchronization signals (control signals)

(6) Explain registers organization of 8085. OR Explain Internal Operation perform by the microprocessor

The 8085 can perform a number of internal operations. Such as: storing data, Arithmetic & Logic operations, testing for condition, etc. To perform these operations, the microprocessor needs an internal architecture similar to the following:



Registers

Six general purpose 8-bit registers: B, C, D, E, H, L

They can also be combined as register pairs to perform 16-bit operations: BC, DE, and HL

Registers are programmable (data load, move, etc.)

Accumulator

Single 8-bit register that is part of the ALU

Used for arithmetic / logic operations – the result is always stored in the accumulator.

Flag Bits

Indicate the result of condition tests.

Carry, Zero, Sign, Parity, etc.

Conditional operations (IF / THEN) are executed based on the condition of these flag bits.

The Program Counter (PC)

This is a register that is used to control the sequencing of the execution of instructions.

This register always holds the address of the next instruction.

Since it holds an address, it must be 16 bits wide.

The Stack pointer

The stack pointer is also a 16-bit register that is used to point into memory.

The memory this register points to be a special area called the stack.
The stack is an area of memory used to hold data that will be retrieved soon.
The stack is usually accessed in a Last in First out (LIFO) fashion.

(7) Define following terms: Instruction, Machine Cycle, Opcode, Oprand & Instruction Cycle.

Instruction:

Instruction is the command given by the programmer to the Microprocessor to Perform the Specifictask. For example, transfer a data, to do addition etc.

Machine Cycle:

Machine cycle is the time required to transfer data to or from memory or I/O devices. Each read or writes operation constitutes a machine cycle. The instructions of 8085 require 1–5 machine cycles containing 3–6 clocks.

The 1st machine cycle of any instruction is always an Op code fetching cycle in which the processor decides the nature of instruction. It is of at least 4-clocks. It may go up to 6-Clocks.

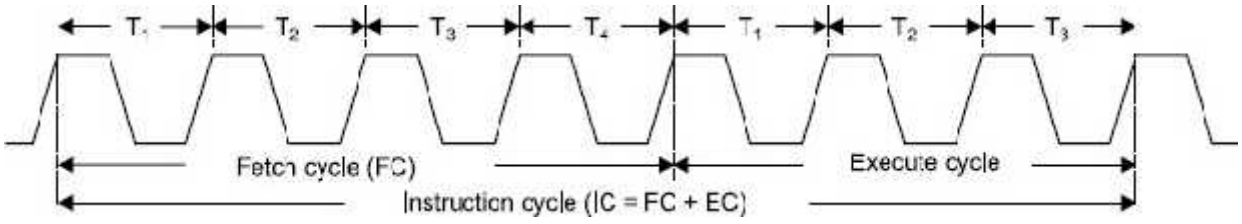
Instruction Cycle:

An instruction cycle is defined as the time required for fetching and executing an instruction.

For executing any program, basically 3-steps are followed sequentially that is Fetch, Decode and Execute.

The time taken by the μP in performing the fetch operations is called fetch cycle (Opcode fetch).The time taken by the μP in performing the execution operations is called execute cycle

Thus, sum of the fetch and execute cycle is called the instruction cycle as indicated in Fig



Instruction Cycle (IC) = Fetch cycle (FC) + Execute Cycle (EC)

Op code:

Operation Perform by the microprocessor is called Op code.

Operand:

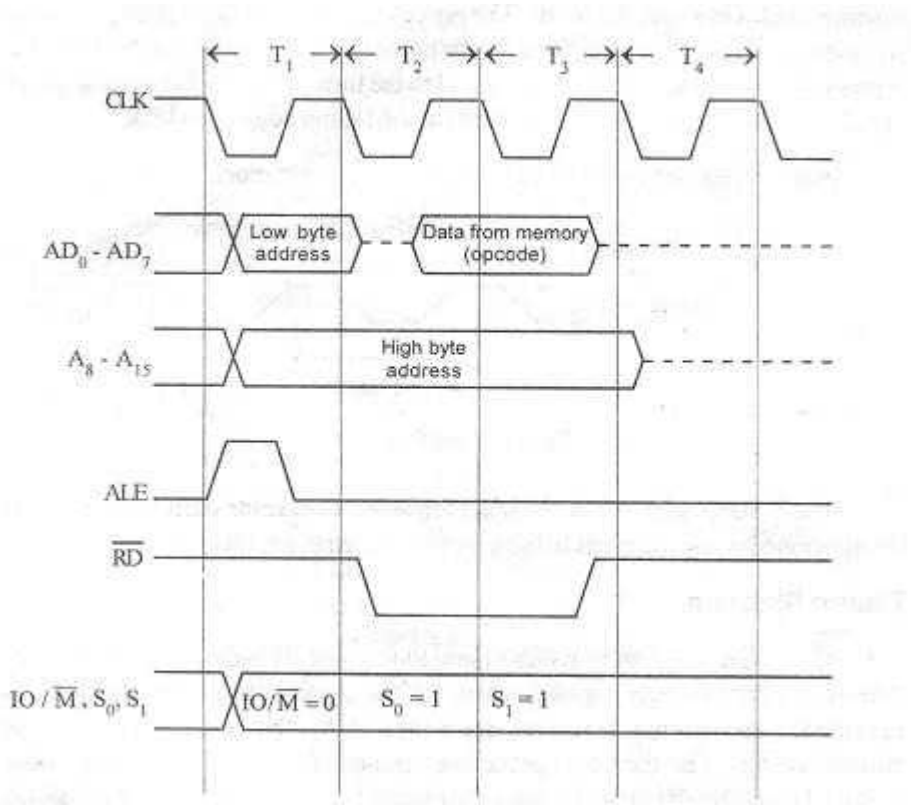
The Data on which Microprocessor perform operation is called Operand.

(8) Draw and explain the Timing Diagram for Opcode Fetch operation.

Each instruction of the processor has one byte Opcode. The Opcode are stored in memory. So, the processor executes the Opcode fetch machine cycle to fetch (Read) the Opcode from memory. Hence, every instruction starts with Opcode fetch machine cycle.

The time taken by the processor to execute the Opcode fetch cycle is 4T or 6T.In this time, the first, 3 T-states are used for fetching the Opcode from memory and the remaining T-states are used for internal operations by the processor.

Timing diagram of Opcode fetch cycle is shown in figure.



T1 State: - In the T1 state, the microprocessor send the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines. ALE is send high to enable the address latch. The other control signals are asserted as follows. IO/$\overline{M}$=0, S0=1, S1=1

T2 State:-In the T2-state, the microprocessor send the RD' to the memory. When RD' asserted to low the memory is enabled for placing the data on the data bus. The time allowed for memory to output the data is the time during which read remains low.

T3 State:-In third T3-state, the read signal is asserted high. On the rising edge of read signal the data is latched into microprocessor other control signals remains in the same state until the next machine cycle.

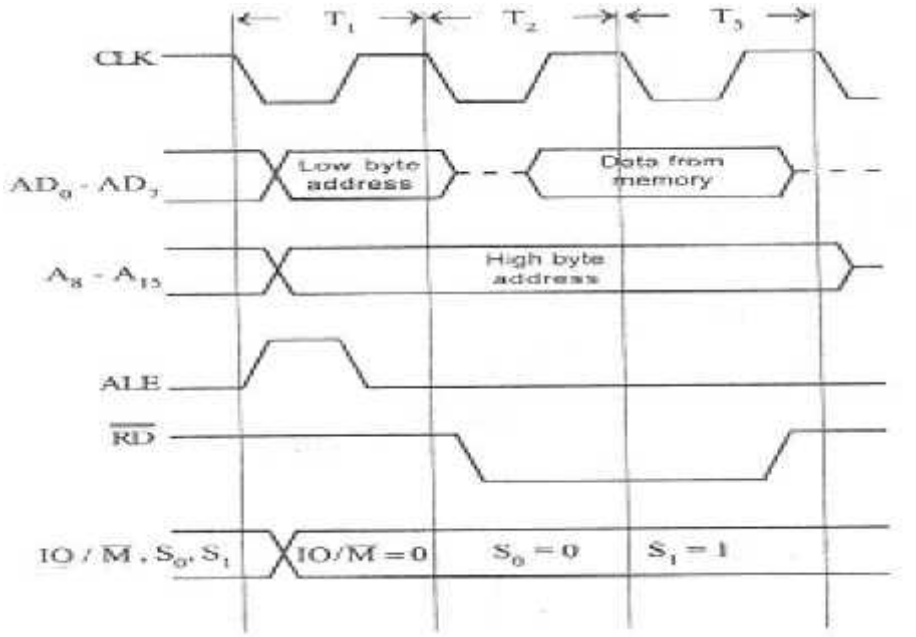
T4 State:-The T4-state is used by the processor for internal operations to decode the instruction and encode into various machine cycles, and also for completing the task specified by l byte instructions. During this cycle the address and data bus will be in high impedance state.

(9) Explain memory read and Write operation with help of timing diagram.

Memory read Operation:-

The memory read machine cycle is executed by the processor to read a data byte from memory. Theprocessor takes 3T states to execute this cycle.

Timing diagram of Memory Read cycle is shown in figure.



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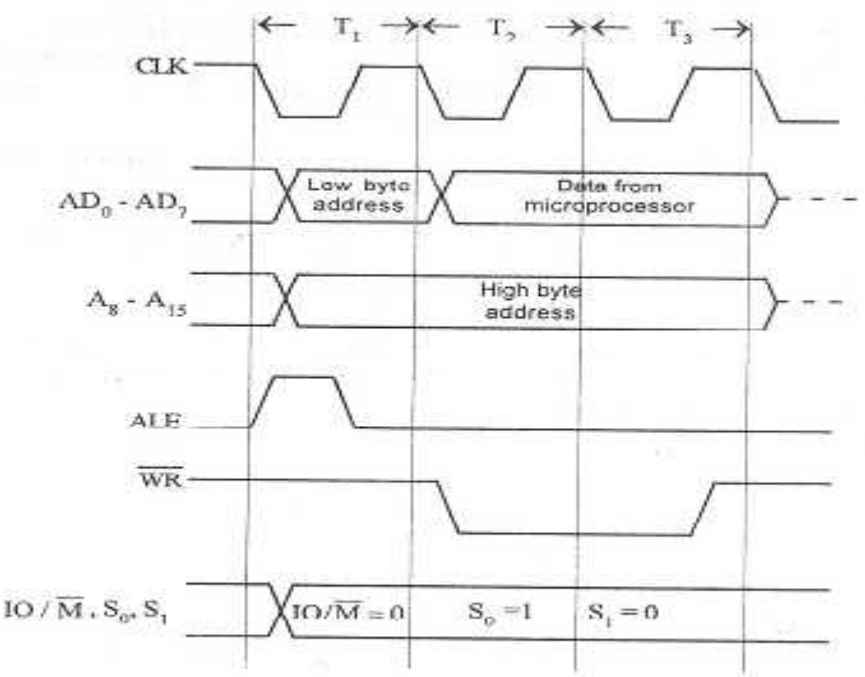
T2 State:-In the T2-state, the microprocessor send the $\overline{RD}$ to the memory. When RD is asserted to low the memory is enabled for placing the data on the data bus. The time allowed for memory to output the data is the time during which read remains low.

T3 State:-In third T3-state, the read signal is asserted high. On the rising edge of read signal the data is latched into microprocessor other control signals remains in the same state until the next machine cycle.

Memory write Operation:-

The memory write cycle is executed by processor to write a data byte in a memory location. The processor takes 3T states to execute this machine cycle. The timing of various signals during memory write cycle is shown infig below.



(RD will be high ; READY is tied high either permanently or temporarily in the system)

Memory write machine cycle of 8085

T1 State: - In the T1 state, the microprocessor send the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines. ALE is asserted high to enable the address latch. The other control signals are asserted as follows. IO/$\overline{M}$=0, S0=1, S1=0

T2 State:-In the T2-state, the microprocessor send the WR The memory. When WR is asserted to low the memory is enabled for placing the data on the data bus. The time allowed for memory to write the data is the time during which WR remains low.

T3 State:-In third T3-state, the write signal is asserted high. On the rising edge of write signal the datais write to memory other control signals remains in the same state until the next machine cycle.

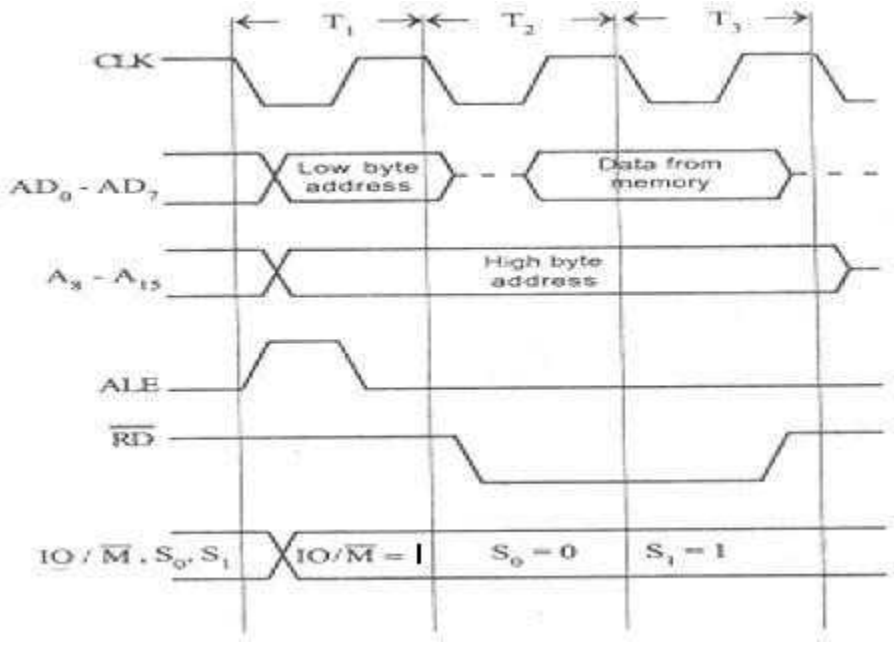
(10)Explain I/O read and I/O Write operation with help of timing diagram.

I\O read Operation:-

I\O read machine cycle is executed by the processor to read a data byte from input device.

Theprocessor takes 3T states to execute this cycle.

Timing diagram of I\O Read cycle is shown in figure.



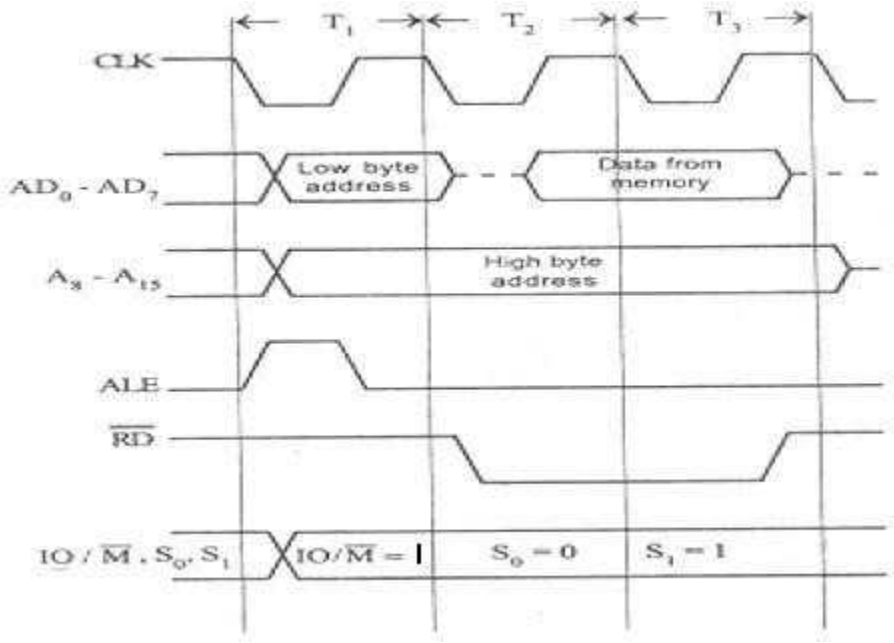
T1 State: - In the T1 state, the microprocessor send the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines. ALE is asserted high to enable the address latch. The other control signals are asserted as follows. IO/$\overline{M}$=1, S0=0, S1=1

T2 State:-In the T2-state, the microprocessor send the RD to the memory. When RD is asserted to low the memory is enabled for placing the data on the data bus. The time allowed for memory to output the data is the time during which read remains low.

T3 State:-In third T3-state, the read signal is asserted high. On the rising edge of read signal the data is latched into microprocessor other control signals remains in the same state until the next machine cycle.

I\O write Operation:-

The I\O write cycle is executed by processor to write a data byte in a memory location. The processor takes 3T states to execute this machine cycle. The timing of various signals during memory write cycle is shown in fig below.



T1 State: - In the T1 state, the microprocessor send the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines. ALE is asserted high to enable the address latch. The other control signals are asserted as follows. IO/M' =1, S0=1, S1=0

T2 State:-In the T2-state, the microprocessor send the WR to the memory. When WR' is asserted to low the memory is enabled for placing the data on the data bus. The time allowed for memory to write the data is the time during which WR' remains low.

T3 State:-In third T3-state, the write signal is asserted high. On the rising edge of write signal the data is write to memory other control signals remains in the same state until the next machine cycle.