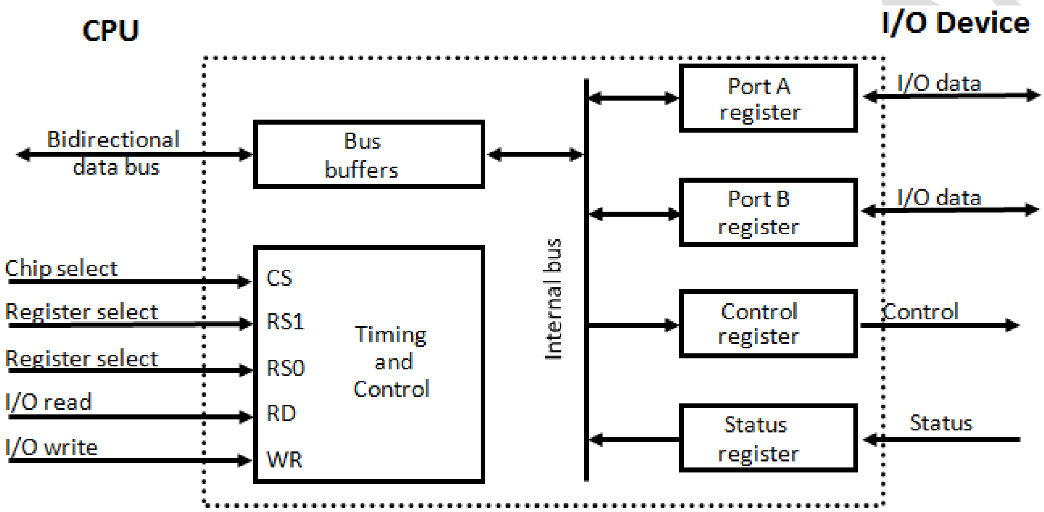
Unit :V Input-Output Organization

5.1. Explain I/O interface

- It consists of two data registers called ports, a control register, a status register, bus buffers, and timing and control circuit.
- The interface communicates with the CPU through the data bus.
- The chip select and register select inputs determine the address assigned to the interface.
- The I/O read and writes are two control lines that specify an input or output,respectively.
- The four registers communicate directly with the I/O device attached to the interface.
- A command is passed to the I/O device by sending a word to the appropriate interface register.
- The control register receives control information from the CPU.



CS	RS1	RS0	Register Selected
0	X	X	None: data bus in high impedance
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register

- For example, port A may be defined as an input port and port B as an output port.
- The interface registers communicate with the CPU through the bidirectional data bus.
- The address bus selects the interface unit through the chip select and the two registerselect inputs.
- The two register select inputs RS1 and RS0 are usually connected to the two leastsignificant lines of the address bus.
- These two inputs select one of the four registers in the interface as specified in the table accompanying the diagram.
- The content of the selected register is transfer into the CPU via the data bus when the I/O read signal is

enables.

- ✓ The CPU transfers binary information into the selected register via the data bus when the I/O write input is enabled.

5.2. Differentiate various Modes of Data Transfer with I/O

- ✓ Data transfer to and from peripherals may be handled in one of three possible modes.

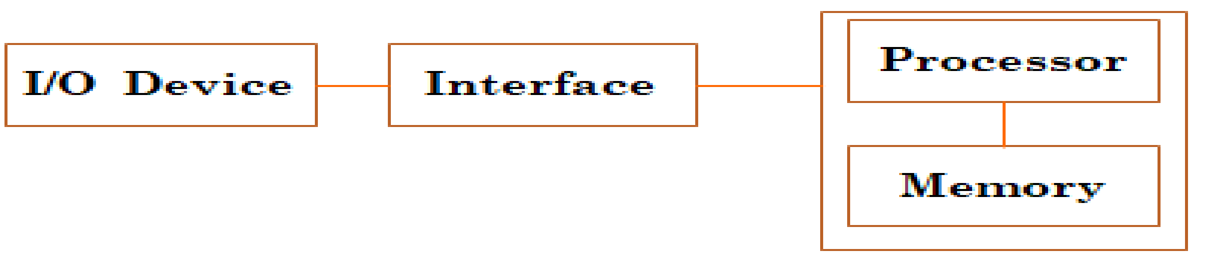
1) Programmed I/O

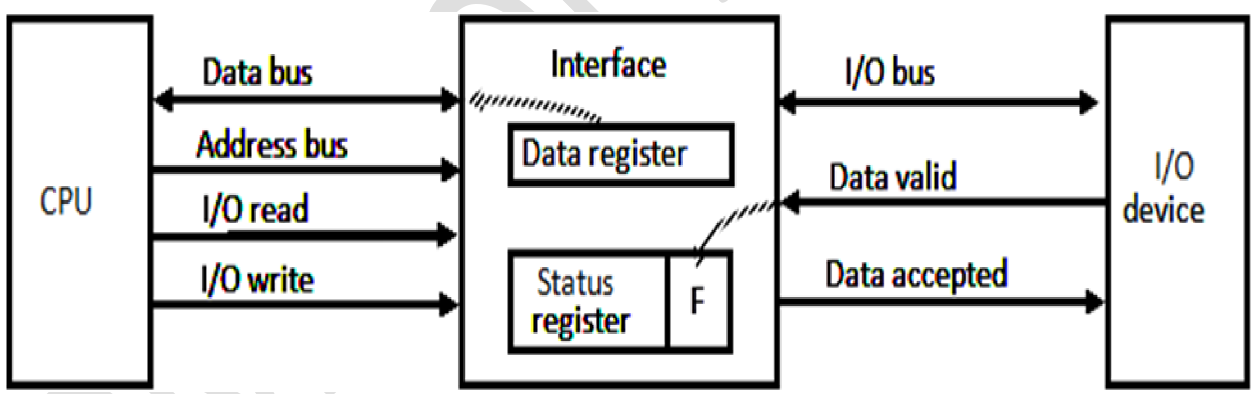
2) Interrupt initiated I/O

3) Direct Memory Access(DMA)

Programmed I/O

- ✓ The I/O device does not have direct access to memory.
- ✓ A transfer from I/O device to memory require the execution of several instruction by CPU(device to CPU and CPU to memory, no of words transferred)





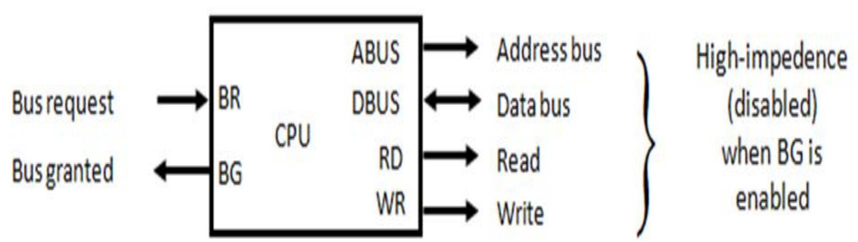
- ✓ When a byte of data is available, the device places it in the I/O bus and enables its data valid line.
- ✓ The interface accepts the byte into its data register and enables the data accepted line.
- ✓ The interface sets a bit in the status register that we will refer to as an F or "flag" bit.
- ✓ The device can now disables the data valid line.
- ✓ Then reading the status register into a CPU register and check the value of the flag bit .
- ✓ If the flag is equal to 1, the CPU reads the data from the data register.
- ✓ The flag bit is then cleared to 0 by CPU or Interface(depends o IC)
- ✓ Then Interface disable the data accepted line and the device can transfer the next data byte.

Interrupt Initiated I/O.

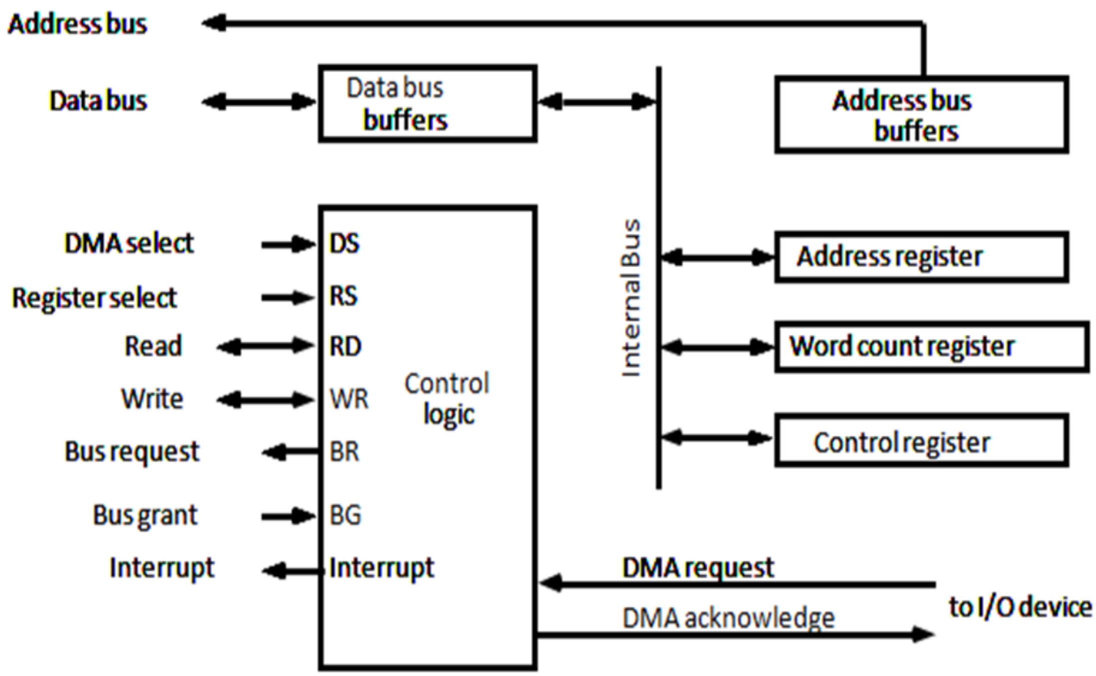
- ✓ In programmed initiated, CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer.
- ✓ It keeps the processor busy without need.
- ✓ It can be avoided by using an interrupt facility .
- ✓ When the data are available from devices, interface issues an interrupt request signal.
- ✓ In the meantime CPU can proceed to execute another program.
- ✓ The interface meanwhile keeps monitoring the device.
- ✓ When the interface determines that the device is ready for data transfer, it generates an interrupt request to the computer.
- ✓ Upon detecting the external interrupt signal, CPU stops the task, branches to the service program to process I/O and then return to the task it was originally *performing*.

DMA(Direct Memory Access)

- ✓ The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of the CPU.
- ✓ Removing the CPU from the path and peripheral device manage the buses directly will improve the speed of transfer.
- ✓ This transfer technique is called DMA.
- ✓ A DMA controller takes over the buses to manage the transfer directly between the I/O devices and memory.
- ✓ BR is used by DMA Controller to request CPU to relieve control of buses.
- ✓ BR is active, then CPU place address bus, data bus, read and write line into high impedance state.



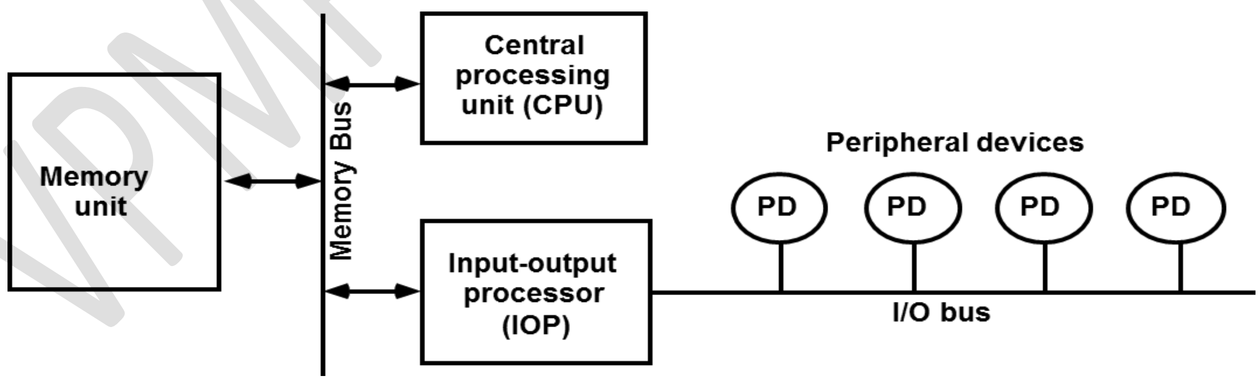
- ✓ The CPU activate the BG to inform DMA that buses are in high impedance state.
- ✓ DMA takes the control of buses and conduct memory transfer.
- ✓ When the DMA terminates the transfer, it disable the bus request line(BR).
- ✓ CPU disable the BG.



- ✓ The register in the DMA are selected by the DS (DMA select) and RS (register select) inputs.
- ✓ The RD (read) and WR (write) inputs are bidirectional.
- ✓ When the BG is 0, the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA registers.
- ✓ When BG= 1, the CPU relieve the buses and the DMA can communicate directly with the memory
- ✓ The word count register holds the number of words to be transferred.

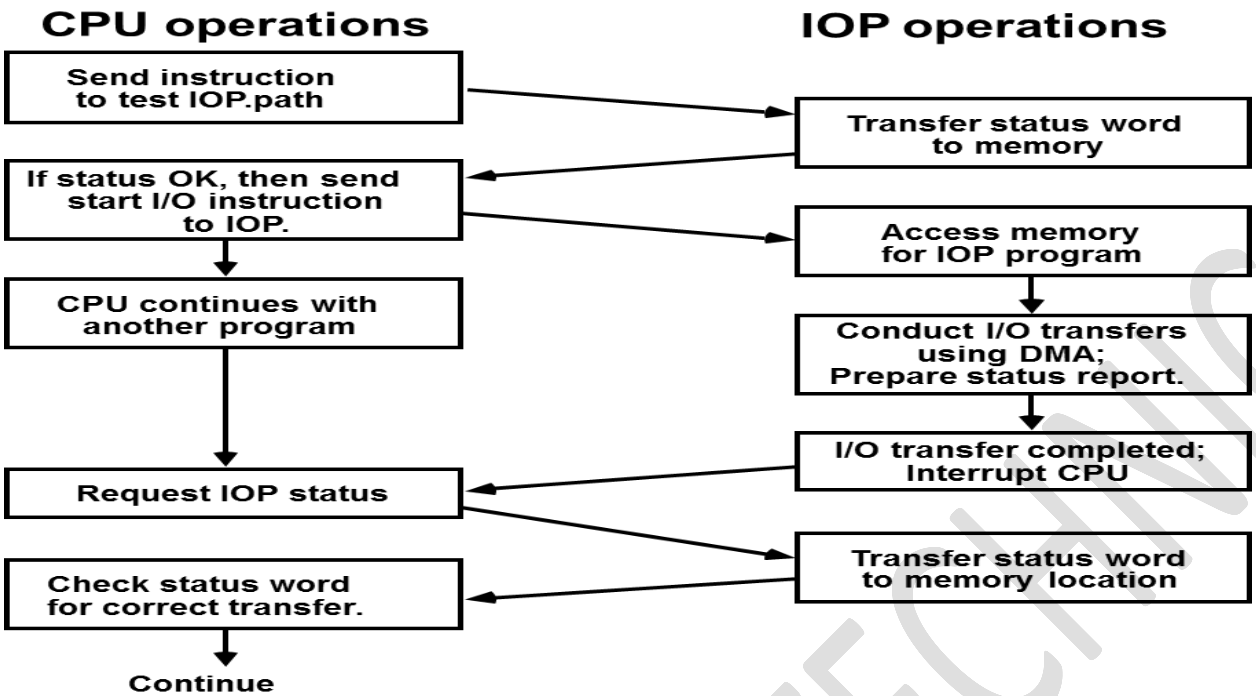
5.3. Describe Input-Output Processor (IOP)

- ✓ Instead of having each Interface communicate with CPU, computer may have one or more external processor.
- ✓ Each processor communicates directly with I/O devices.
- ✓ IOP may be classified as a processor with direct memory access capability that communicates with I/O devices.



- ✓ IOP provides a path for transfer of data between various peripheral devices and the memory unit.
- ✓ IOP operates independent of the CPU.

5.4. Describe CPU-IOP communication



- ✓ CPU send an instruction to test the IOP path.
- ✓ The IOP responds by inserting a status word in memory for CPU.
- ✓ Status word indicate the condition of the IOP and I/O device(IOP overload condition, device busy, device ready)
- ✓ The CPU check the status word in memory to decide what to do.
- ✓ If status is OK, send start I/O instruction to IOP.
- ✓ Now CPU is continue with another program while IOP is busy with I/O program.
- ✓ When IOP terminates the execution, it send interrupt request to CPU.
- ✓ CPU send request for IOP Status.IOP send status report. It indicates the transfer has been completed or if any error occurs during the transfer.CPU check status word for correct transfer.